21 NOV 95 16:24:44 U.S. Patent & Trademark Office P0004

US PAT NO: 5,146,546 [IMAGE AVAILABLE] L3: 2 of 2
word identifying the symbol. The printer includes a microprocessor control circuit that receives input data including a code word identifying a symbol to be printed from an input device. The microprocessor control circuit includes a direct memory access controller for controlling the transfer of data from the symbol memory to an. . .

DETDESC:

DETD(15)

The device select sequencer 150 of the memory controller 46 is essentially a three-bit ring counter that is clocked on a read signal from the DMAC 28 if the JIS registers 40 and 42 are enabled and the symbol. . .

```
=> s l2 and (counter (5a) clock?)/ab
         18853 COUNTER/AB
         16405 CLOCK?/AB
          1588 (COUNTER (5A) CLOCK?)/AB
L4           7 L2 AND (COUNTER (5A) CLOCK?)/AB

=> d l4 kwic 1-7
```

US PAT NO: 5,274,764 [IMAGE AVAILABLE] L4: 1 of 7
US-CL-CURRENT: 395/250; 364/236.2, 238.3, 239, 239.1, 239.6, 239.7, 248.1, 249.4, 271.9, DIG.1

ABSTRACT:
A . . . signal and left/right clock signal, an optical disk ROM decoder for decoding and transmitting the data from the processor, a microprocessor for controlling the whole system, and a data input controller for controlling the output of the digital signal processor. The data input controller includes a clock generator, a counter, a first control signal generator, an AND gate, a stop point detector for shifting the serial data of the digital. . .

US PAT NO: 5,107,523 [IMAGE AVAILABLE] L4: 2 of 7
US-CL-CURRENT: 377/2; 327/18, 44; 371/62; 377/28; 395/182.22

ABSTRACT:
An input to the control unit of a microprocessor places the microprocessor in a WAIT condition whenever the input clock frequency is determined to be greater than a predetermined maximum value. An. . . time interval between successive clock pulses is less than a value corresponding to a cut-off frequency. To assure that the microprocessor is not placed in a WAIT state by an occasional "glitch" on the clock input, the kill signal applied to the microprocessor control unit is provided from a four-bit counter. If the Schmitt trigger generates a kill signal on eight consecutive clock cycles, the counter output changes state and sequencing of microcode by the control unit is suspended.

US PAT NO: 4,982,404 [IMAGE AVAILABLE] L4: 3 of 7
US-CL-CURRENT: 371/62; 364/230.2, 232.8, 242.4, 244.6, 267, 267.4, 267.9, 268.1, 268.3, 268.8, 280, 280.2, 280.8, DIG.1; 371/61; 395/185.08

ABSTRACT:
In a system controller having multiple parts including a microprocessor, a main program for execution upon the microprocessor, and at least one clock
16:26:47 COPY AND CLEAR PAGE, PLEASE

INPUT:

US PAT NO: 4,982,404 [IMAGE AVAILABLE] L4: 3 of 7
interrupt handler portion, a method and apparatus for insuring proper operation comprised of providing a. . . The hardware watchdog timer reinitializes the main program in the event that the main program fails to respond to the clock interrupt handler and the delay counter reinitializes the main program and the clock interrupt handler in the event that the watchdog timer fails to operate. Therefore,. . .

US PAT NO: 4,809,280 [IMAGE AVAILABLE] L4: 4 of 7
US-CL-CURRENT: 371/62; 364/231, 232.8, 237.2, 237.4, 242, 243, 243.3, 260.4, 260.8, 262.4, 262.9, 264, 264.5, 265, 266, 267, 267.4, 267.9, 270, 270.3, 270.4, 285, DIG.1; 395/185.08

ABSTRACT:
A microcomputer executes a certain system program with a microprocessor according to a certain system clock. The microcomputer includes a watchdog timer circuit provided external to the microcomputer which counts a certain time interval by counting a certain timer clock which is separate from the system clock with a counter for a certain count and, upon completion of the counting, forcibly resets the microprocessor of the microcomputer. The system program of the microprocessor has a step of producing a reset output to the counter before a predetermined time only when the system action. . . the normal period of the timer clock of the watchdog timer circuit, and upon completion of the counting interrupts the microprocessor of the microcomputer. The system program of the microcomputer has a step in which reset output is supplied to the. . .

US PAT NO: 4,434,461 [IMAGE AVAILABLE] L4: 5 of 7
US-CL-CURRENT: 395/733; 364/222.2, 222.3, 222.4, 231, 231.2, 231.3, 232.8, 234, 237.2, 237.4, 237.8, 241.2, 243, 243.7, 244, 244.6, 244.9, 247, 252, 259.9, 284, 284.2, DIG.1; 455/33.1, 73

ABSTRACT:
A unique microprocessor for controlling portable and mobile cellular radiotelephones is architectured to process high speed supervisory signalling, while also minimizing power drain. The architecture of the microprocessor is organized around three buses, a data bus, a register bus and an address bus. Data signals are routed between the various blocks of the microprocessor by selectively interconnecting the three buses in response to control signals provided by ALU and control programmable logic arrays (PLA).. . . PLA's decode program instructions loaded in instruction register (IR) to provide the appropriate control signals for executing each instruction. The microprocessor also includes three general purpose registers, an arithmetic logic unit (ALU) with two temporary registers and zero and carry flags,. . . a temporary program counter register and associated incrementer, and a temporary address register. Because of the unique architecture of the microprocessor, all instructions can be executed in four or less clock cycles. Moreover, the program counter register, general purpose registers and zero and carry flags are duplicated, and, during interrupts, the microprocessor switches over to the duplicate program counter register, duplicate general purpose registers and duplicate zero and carry flags. As a. . . counter register, general purpose registers and zero and carry flags and their duplicates. Since instruction execution time is minimized, the microprocessor can be operated at slower speeds to conserve power drain, while maintaining the through-put necessary for accommodating high-speed, cellular type supervisory signalling. Thus, a microprocessor embodying the present invention can be advantageously utilized in any application where both low power consumption and fast data
16:27:18 COPY AND CLEAR PAGE, PLEASE

INPUT:

21 NOV 95 16:27:45 U.S. Patent & Trademark Office P0006

US PAT NO: 4,434,461 [IMAGE AVAILABLE] L4: 5 of 7
manipulation. . .

US PAT NO: 4,161,787 [IMAGE AVAILABLE] L4: 6 of 7
US-CL-CURRENT: 395/550; 364/933, 934, 934.1, 934.3, 940, 940.2, 941, 941.5, 942.7, 949.3, 950, 950.4, DIG.2; 377/20, 26; 395/733

ABSTRACT:
A programmable timer module (PTM) is provided as a component of a microprocessor system in order to generate and measure varying time intervals under program control. The programmable timer module includes, in one. . . register and an 8-bit control register each of which may be coupled to an 8-bit bidirectional data bus of a microprocessor system. Selection circuitry is provided which permits the microprocessor to select either the control register or the status register. Information can be written into the control register; the operation. . . generates an interrupt signal and sets an appropriate interrupt bit in the status register, and also resets that counter. The counter continues counting at the appropriate clock rate after the interrupt so that time since the interrupt may be determined by the microprocessor. The outputs of the three counters can be selected as outputs of the programmable timer module.

US PAT NO: 4,144,561 [IMAGE AVAILABLE] L4: 7 of 7
US-CL-CURRENT: 395/800; 364/232.7, 232.8, 240.1, 243, 243.3, 244, 244.3, 244.6, 252, 254, 254.5, 259, 259.1, 271, DIG.1

ABSTRACT:
The chip topography of an MOS microprocessor chip. The chip architecture includes an internal data bus and an internal address bus. Input/output circuitry is located along the. . . in the lower left hand corner of the chip. The ROM contains instruction words for defining the operation of the microprocessor. A data storage area which includes a RAM is located in the upper left hand corner of the chip and. . . bus for receiving instruction words from the program storage area and for generating commands which define the operation of the microprocessor in response to the instruction words. A clock/T-counter is located in the lower right hand corner and is used for synchronizing data signal flow in the micrprocessor. A. . .

```
=> s l1 and (microprocessor? (5a) counter (5a) clock?)
         63992 MICROPROCESSOR?
        210468 COUNTER
          238405 CLOCK?
          254 MICROPROCESSOR? (5A) COUNTER (5A) CLOCK?
L5         28 L1 AND (MICROPROCESSOR? (5A) COUNTER (5A) CLOCK?)

=> d l5 kwic 1-28
```

US PAT NO: 5,440,749 [IMAGE AVAILABLE] L5: 1 of 28
US-CL-CURRENT: 395/800; 364/232.8, 244.3, 926.6, 931, 937.1, 965.4, DIG.1, DIG.2

SUMMARY:

BSUM(20)

In a further aspect of the invention, the microprocessor system has a ring counter variable speed system clock connected to the central processing unit. The central processing unit and the ring counter variable speed system 16:30:04 COPY AND CLEAR PAGE, PLEASE

INPUT: /

21 NOV 95 16:30:12 U.S. Patent & Trademark Office P0007

US PAT NO: 5,440,749 [IMAGE AVAILABLE] L5: 1 of 28

BSUM(20)
clock are provided. . .

CLAIMS:

CLMS(23)

23. The microprocessor system of claim 9 in which said microprocessor system is configured to operate at a variable clock speed; said microprocessor system additionally comprising a ring counter variable speed system clock connected to said central processing unit, said central processing unit and said ring counter variable speed system clock being provided. . .

US PAT NO: 5,396,599 [IMAGE AVAILABLE] L5: 2 of 28
US-CL-CURRENT: 395/280, 175

DETDESC:

DETD(175)

The . . . and WC0 may be used to allow more than seven wait states to be inserted into a bus cycle of microprocessor 1. The counter implemented by Ready/Clock generator 25 may count not from the number of wait states down to zero but, say, from 1 up to. . .

US PAT NO: 5,295,257 [IMAGE AVAILABLE] L5: 3 of 28
US-CL-CURRENT: 395/550

DETDESC:

DETD(3)

As shown in FIG. 3, each clock, such as clock 10-1, has a microprocessor 20, an M-counter 22 which stores the number of pulses, a C-counter 24 which stores a polling request signal, an S-counter which stores. . .

DETDESC:

DETD(13)

The . . . block 50, the microprocessor 20 will inquire, decision block 52, if polling result signals S have been received from other clocks. If so, the microprocessor 20 will increment the S-counter 28 for each received polling result signal received, as indicated by block 54. The content of the S-counter 28 is. . .

US PAT NO: 5,287,411 [IMAGE AVAILABLE] L5: 4 of 28
US-CL-CURRENT: 381/36; 340/902, 907; 381/41; 395/2.4

DETDESC:

DETD(29)

such . . . incorporated in chips such as the Intel MCS51 family of chips,

INPUT:

21 NOV 95 16:30:23 U.S. Patent & Trademark Office P0008

US PAT NO: 5,216,751 [IMAGE AVAILABLE] L5: 5 of 28
US-CL-CURRENT: 395/27; 364/728.01; 395/11

DETDESC:

DETD(12)

While . . . terminal 34, for further processing by an external controller such as a microprocessor (not shown). Upon command from the external microprocessor, counter 74 is incremented thereby clocking each shift register 68 of neuron slices 14-24 and shifting the 8-bit feedforward outcome of each neuron slice one position. . .

US PAT NO: 5,208,900 [IMAGE AVAILABLE] L5: 6 of 28
US-CL-CURRENT: 395/27, 11, 800

DETDESC:

DETD(12)

While . . . terminal 34, for further processing by an external controller such as a microprocessor (not shown). Upon command from the external microprocessor, counter 74 is incremented thereby clocking each shift register 68 of neuron slices 14-24 and shifting the 8-bit feedforward outcome of each neuron slice one position. . .

US PAT NO: 5,168,556 [IMAGE AVAILABLE] L5: 7 of 28
US-CL-CURRENT: 395/891; 364/921.8, 921.9, 927.92, 927.93, 927.95, 927.98, 939, 939.5, 942.7, 942.8, 947, 947.1, 950, 950.3, 950.5, DIG.2

CLAIMS:

CLMS(5)

5. A circuit as claimed in claim 4 wherein said means for generating first prompter signals for said microprocessor has a transmission clock counter counting repeatedly and continuously with a transmission clock and generating a first prompter signal when a preset maximum counter reading. . .

CLAIMS:

CLMS(6)

6. A circuit as claimed in claim 4 wherein said means for generating second prompter signals for said microprocessor has a reception clock counter counting repeatedly and continuously with a reception clock at a change in said message and generating a second prompter signal. . .

CLAIMS:

CLMS(7)

7. . . .
comprising an information storage registering circuit for presetting said transmission circuit, said information storage registering circuit is connected with said microprocessor, a transmission clock counter

INPUT:

21 NOV 95 16:30:36 U.S. Patent & Trademark Office P0009

US PAT NO: 5,168,556 [IMAGE AVAILABLE] L5: 7 of 28

CLMS(7)
means for counting a transmission clock and a transmission logic section for transmitting said first data bit stream and said control bit stream being dependent on. . . includes outputs for control lines and a data transmission line, and is connected via a transmitter prompter line to said microprocessor;
wherein said transmission clock counter means, having a presettable maximum counter reading, is connected to said transmission clock line;
a reception circuit, connected with said bit stream converter, comprising a message information output circuit connected with said microprocessor, a reception clock counter connected to a reception clock line, and a reception logic circuit; and
wherein said reception logic circuit includes inputs for a reception data line and message. . .

US PAT NO: 5,008,940 [IMAGE AVAILABLE] L5: 8 of 28
US-CL-CURRENT: 395/2.33; 381/36; 395/2.14

DETDESC:

DETD(42)

The . . . master clock input from the master clock 26 on line 59, and may be reset via line 56 from the microprocessor 35. The negative slope counter 45 receives the master clock input on line 60, and may be reset via line 51 by microprocessor 35.

US PAT NO: 4,930,101 [IMAGE AVAILABLE] L5: 9 of 28
US-CL-CURRENT: 395/106; 364/921.8, 927.2, 930, 930.7, 934, 942.7, 948.4, 948.5, 948.91, 965, 965.76, 965.79, DIG.2; 395/750; 400/53

DETDESC:

DETD(3)

A . . . METER PACKAGE 1, such as in the microprocessor. From these control, data, and input signals and by reference to the clock signal the MICROPROCESSOR 2 CALCULATES the counter variables (1) HOURS ON, (2) PRINT HOURS, (3) PRINTED LINES, and (4) REMAINING RIBBON LIFE. These quantities and others are. . .

US PAT NO: 4,912,708 [IMAGE AVAILABLE] L5: 10 of 28
US-CL-CURRENT: 395/185.08; 371/62

DETDESC:

DETD(9)

The . . . of a 74HC4060 14-bit counter shown at 114 whose Q13 output is inverted and returned to the NMI of the microprocessor 104. The counter 114 clock is derived from an eight kilohertz pulsed signal. The allocated time out interval is therefore fixed at 0.512 seconds, allowing. . .

US PAT NO: 4,908,790 [IMAGE AVAILABLE] L5: 11 of 28
16:30:38 COPY AND CLEAR PAGE, PLEASE

INPUT:

21 NOV 95 16:31:01 U.S. Patent & Trademark Office P0010

US PAT NO: 4,908,790 [IMAGE AVAILABLE] L5: 11 of 28
US-CL-CURRENT: 395/182.12; 307/66; 364/931, 934, 934.71, 942.7, 943.9, 943.91, 944.2, 944.3, 946.2, 947, 947.1, 947.2, 948.4, 948.5, 950, 950.2, DIG.2; 365/229; 395/750

CLAIMS:

CLMS(1)

What . . .
said microcomputer or microprocessor has issued a sequence of predetermine commands, and switches to a second logic state when a counter in said microcomputer or microprocessor counts a predetermined number of clock cycles of said microcomputer or microprocessor after said counter has been reset; and
(b) switching means for operatively connecting said backup battery voltage to said output terminal when said voltage. . .

CLAIMS:

CLMS(3)

3. . . .
microcomputer or microprocessor issues a sequence of predetermined commands, and
said latch circuit being switchable to said second state when a counter circuit in said microcomputer or microprocessor counts a predetermined number of clock cycles of said microcomputer or microprocessor after said counter has been reset; and
isolating said backup battery input terminal from said power supply output terminal when said backup battery. . .

CLAIMS:

CLMS(4)

4. . . .
input, and to provide a corresponding output;
a counter circuit;
a latch circuit which switches to a second logic state when a counter in said microcomputer or microprocessor counts a predetermined number of clock cycles of said microcomputer or microprocessor after said counter has been reset, and which can also be switched to a first logic state; and
a switching circuit which
connects said. . .

US PAT NO: 4,860,289 [IMAGE AVAILABLE] L5: 12 of 28
US-CL-CURRENT: 395/182.13; 371/62; 395/185.08

SUMMARY:

BSUM(23)

Preferably, . . . slave circuit. An external crystal may be used to set the frequency of the oscillator, whether within or without the microprocessor. The counter utilizes the clock signal to count the
16:31:02 COPY AND CLEAR PAGE, PLEASE

INPUT: //////

```
=> d his

     (FILE 'USPAT' ENTERED AT 16:21:54 ON 21 NOV 95)
               SET PAGELENGTH 62
               SET LINELENGTH 78
L1         26522 S 395/?/CCLS
L2          1403 S L1 AND (MICROPROCESSOR?)/AB
L3             2 S L2 AND (RING (5A) COUNTER (5A) CLOCK?)
L4             7 S L2 AND (COUNTER (5A) CLOCK?)/AB
L5            28 S L1 AND (MICROPROCESSOR? (5A) COUNTER (5A) CLOCK?)

=> s l1 and (microprocessor? (5a) variable (5a) clock?)
         63992 MICROPROCESSOR?
        268077 VARIABLE
        238405 CLOCK?
            17 MICROPROCESSOR? (5A) VARIABLE (5A) CLOCK?
L6           6 L1 AND (MICROPROCESSOR? (5A) VARIABLE (5A) CLOCK?)

=> d l6 kwic 1-6

US PAT NO:      5,440,749 [IMAGE AVAILABLE]              L6: 1 of 6
US-CL-CURRENT: 395/800; 364/232.8, 244.3, 926.6, 931, 937.1, 965.4, DIG.1,
                 DIG.2

SUMMARY:

BSUM(20)

 In a further aspect of the invention, the microprocessor system has a ring
counter variable speed system clock connected to the central processing
unit. The central processing unit and the ring counter variable speed system
clock are provided. . .

CLAIMS:

CLMS(23)

 23. The microprocessor system of claim 9 in which said microprocessor system
is configured to operate at a variable clock speed; said microprocessor
system additionally comprising a ring counter variable speed system clock
connected to said central processing unit, said central processing unit. .
.

US PAT NO:      5,339,395 [IMAGE AVAILABLE]              L6: 2 of 6
US-CL-CURRENT: 395/310; 364/232.9, 239.7, 247.4, 260.1, 270.5, 271, DIG.1;
                 370/91

DETDESC:

DETD(140)

 When the host microprocessor 12 uses asynchronous bus control, data
transfers between the bus interface 10 and the host microprocessor 12
16:33:14 COPY AND CLEAR PAGE, PLEASE
```

INPUT:

21 NOV 95 16:33:27 U.S. Patent & Trademark Office P0012

US PAT NO: 5,339,395 [IMAGE AVAILABLE] L6: 2 of 6

DETD(140)
generally require a variable number of CLK clock cycles, which is unlike the one data byte per clock period transfers that occur with synchronous bus control. To indicate. . .

DETDESC:

DETD(163)

When . . . also waits in operating states to accommodate data transfers between the host microprocessor and the interface that may require a variable number of host microprocessor clock cycles to complete (between access wait state 4). In addition, the interface notifies the host microprocessor when a data transfer. . .

US PAT NO: 5,319,771 [IMAGE AVAILABLE] L6: 3 of 6
US-CL-CURRENT: 395/550; 364/270, 270.2, DIG.1

CLAIMS:

CLMS(1)

What is claimed is:

1. A computer system having a variable frequency microprocessor clock generator, said computer system comprising:
a central processor unit (CPU) comprising a microprocessor, wherein said microprocessor generates a plurality of. . .

CLAIMS:

CLMS(4)

4. A computer system having a variable frequency microprocessor clock generator, said computer system comprising:
a central processor unit (CPU) comprising a microprocessor, wherein said microprocessor generates a plurality of. . .

US PAT NO: 4,819,164 [IMAGE AVAILABLE] L6: 4 of 6
TITLE: Variable frequency microprocessor clock generator
US-CL-CURRENT: 395/550; 364/232.8, 270, 270.1, 270.2, 271, 271.1, DIG.1

US PAT NO: 4,761,763 [IMAGE AVAILABLE] L6: 5 of 6
US-CL-CURRENT: 395/286; 364/DIG.2

SUMMARY:

BSUM(11)

In . . . rate that is higher than nominal. This is achieved by providing the UART of the data unit with a dynamically variable clock. When the microprocessor of the data unit determines that the received data is at a rate above nominal, the local clock rate is. . .

US PAT NO: 4,670,837 [IMAGE AVAILABLE] L6: 6 of 6
16:33:29 COPY AND CLEAR PAGE, PLEASE

INPUT:

21 NOV 95 16:34:09 U.S. Patent & Trademark Office P0013

US PAT NO: 4,670,837 [IMAGE AVAILABLE] L6: 6 of 6
US-CL-CURRENT: 395/550; 327/114; 331/1A; 364/232.2, 242, 273.1, 280, 281, 281.3, DIG.1

ABSTRACT:
The microprocessor unit of a system implemented using metal-oxide-silicon (MOS) technology, is driven by a variable-frequency clock. The microprocessor controls the clock frequency based on the present rate of required microprocessor activity. By driving the microprocessor unit at a lower clock frequency. . .

=>

INPUT:

21 NOV 95 16:34:09 U.S. Patent & Trademark Office P0013

US PAT NO: 4,670,837 [IMAGE AVAILABLE] L6: 6 of 6
US-CL-CURRENT: 395/550; 327/114; 331/1A; 364/232.2, 242, 273.1, 280, 281, 281.3, DIG.1

ABSTRACT:
The microprocessor unit of a system implemented using metal-oxide-silicon (MOS) technology, is driven by a variable-frequency clock. The microprocessor controls the clock frequency based on the present rate of required microprocessor activity. By driving the microprocessor unit at a lower clock frequency. . .

=> s l1 and (ring (5a) counter (5a) clock?)
400493 RING
210468 COUNTER
238405 CLOCK?
1082 RING (5A) COUNTER (5A) CLOCK?
L7 65 L1 AND (RING (5A) COUNTER (5A) CLOCK?)

=> s l7 and microprocessor?/ab
8122 MICROPROCESSOR?/AB
L8 2 L7 AND MICROPROCESSOR?/AB

=> d l8 kwic

US PAT NO: 5,440,749 [IMAGE AVAILABLE] L8: 1 of 2
US-CL-CURRENT: 395/800; 364/232.8, 244.3, 926.6, 931, 937.1, 965.4, DIG.1, DIG.2

ABSTRACT:
A microprocessor (50) includes a main central processing unit (CPU) (70) and a separate direct memory access (DMA) CPU (72) in a single integrated circuit making up the microprocessor (50). The main CPU (70) has a first 16 deep push down tack (74), which has a to item register. . .

SUMMARY:

BSUM(20)

In a further aspect of the invention, the microprocessor system has a ring counter variable speed system clock connected to the central processing unit. The central processing unit and the ring counter variable speed system clock are provided in a single integrated circuit. An input/output interface is connected to exchange coupling control signals, addresses and data with the input/output interface. A second clock independent of the ring counter variable speed system clock is connected to the input/output interface.

DETDESC:

DETD(174)

Most . . . the external world of memory and I/O devices. The CPU 70 executes at the fastest speed possible using the adaptive ring counter clock 430. Speed may vary by a factor of four depending upon temperature, voltage, and process. The external world must be. . .

DETDESC:
16:36:12 COPY AND CLEAR PAGE, PLEASE

INPUT:

21 NOV 95 16:36:22 U.S. Patent & Trademark Office P0014

US PAT NO: 5,440,749 [IMAGE AVAILABLE] L8: 1 of 2

DETD(176)

System . . . writing I/O ports. In some systems (such as calculators) no I/O synchronization at all would be required, and the I/O clock would be tied to the ring counter clock.

CLAIMS:

CLMS(23)

23. . . . in which said microprocessor system is configured to operate at a variable clock speed; said microprocessor system additionally comprising a ring counter variable speed system clock connected to said central processing unit, said central processing unit and said ring counter variable speed system clock being provided in a single integrated circuit, said ring counter variable speed system clock being configured to provide different clock speed to said central processing unit as a result of transistor propagation delays, depending. . .

CLAIMS:

CLMS(24)

24. . . . to exchange coupling control signals, addresses and data between said central processing unit and said input/output interface, and a second clock independent of said ring counter variable speed system clock connected t said input/output interface to provide clock signals for operation of said input/output interface asynchronously from said central processing. . .

=> d his

(FILE 'USPAT' ENTERED AT 16:21:54 ON 21 NOV 95)
SET PAGELENGTH 62
SET LINELENGTH 78

L1	26522	S 395/?/CCLS
L2	1403	S L1 AND (MICROPROCESSOR?)/AB
L3	2	S L2 AND (RING (5A) COUNTER (5A) CLOCK?)
L4	7	S L2 AND (COUNTER (5A) CLOCK?)/AB
L5	28	S L1 AND (MICROPROCESSOR? (5A) COUNTER (5A) CLOCK?)
L6	6	S L1 AND (MICROPROCESSOR? (5A) VARIABLE (5A) CLOCK?)
L7	65	S L1 AND (RING (5A) COUNTER (5A) CLOCK?)
L8	2	S L7 AND MICROPROCESSOR?/AB

=> d l8 kwic 2

US PAT NO: 5,146,546 [IMAGE AVAILABLE] L8: 2 of 2
US-CL-CURRENT: 395/115, 110

ABSTRACT:
A . . . stored in a memory at addresses that are different from the code word identifying the symbol. The printer includes a microprocessor control circuit that receives input data including a code word identifying a symbol to be printed from an input device. The microprocessor control circuit includes a direct memory access controller for controlling the transfer of data from the symbol memory to an. . .
16:36:54 COPY AND CLEAR PAGE, PLEASE

INPUT:

21 NOV 95 16:39:40 U.S. Patent & Trademark Office P0016

US PAT NO: 4,627,002 [IMAGE AVAILABLE] L9: 3 of 3

CLMS(15)
15. A method according to claim 1 including the steps of providing the contour segments as straightline segments, clockwise circular segments, and counter-clockwise circular segments.

=> s l1 and microprocessor?/ab
8122 MICROPROCESSOR?/AB
L10 1403 L1 AND MICROPROCESSOR?/AB

=> s l10 and interface? (5a) clock
165798 INTERFACE?
114654 CLOCK
2505 INTERFACE? (5A) CLOCK
L11 78 L10 AND INTERFACE? (5A) CLOCK

=> s l11 and (i?o (5a) interface? (5a) clock?)
'?' TRUNCATION SYMBOL NOT VALID WITHIN 'I?O'

=> s l11 and (interface? and clock?)/ab
15960 INTERFACE?/AB
16405 CLOCK?/AB
L12 11 L11 AND (INTERFACE? AND CLOCK?)/AB

=> d l12 kwic 1-11

US PAT NO: 5,428,765 [IMAGE AVAILABLE] L12: 1 of 11
US-CL-CURRENT: 395/550; 327/142, 292; 364/483, DIG.1; 370/85.1

ABSTRACT:
The ability to stop a clock in a CMOS peripheral device or other CMOS IC, and reliably restart it based on an asynchronous event, provides the basis for considerable power savings. In a computer system 20 an interface component 10 has a clock restart circuit 100. The restart circuit 100 includes a series of D-type CMOS flip-flops (110, 112, 118) that are initially set in their zero state. A logic OR gate 120 receives the microprocessor clock and the complimentary output of the last flip-flop to provide a reliable, restarted clock signal for the interface component 10 and its peripherals 26.

SUMMARY:

BSUM(1)

This . . . a reliable clock in an electronic system and, in particular, to a method and apparatus for disabling and restarting a clock in an interface device disposed between a microprocessor and a peripheral port, or in any device requiring an internal clock for synchronous operation. . .

DRAWING DESC:

DRWD(3)

FIG. 2 is a schematic diagram of a circuit in the interface component that receives a clock signal from the microprocessor;

DETDESC:
16:43:48 COPY AND CLEAR PAGE, PLEASE

INPUT:

21 NOV 95 16:44:32 U.S. Patent & Trademark Office P0017

US PAT NO: 5,428,765 [IMAGE AVAILABLE] L12: 1 of 11

DETD(2)

With . . . The bus 24 is a standard ISA or PC/AT bus or other system bus. The system bus 24 carries a clock signal, CLK, to the interface component 10. Interface component 10 is a Databook DB86082 PC Card Controller for Notebook Personal Computers, for use with a. . .

DETDESC:

DETD(4)

Turning . . . is the input buffer for interface component 10 and by driving signal NCLKIE to an inactive state, one can eliminate clock transitions on signal RAWCLK within interface component 10. If buffer 116 is implemented with a zero power buffer, then input transitions on line 114 will cause. . .

DETDESC:

DETD(5)

When it is desired to restart the clock inside the interface component 10, it is necessary to change the state of signal NCLKIE to enable the three-state buffer 116 and thereby pass signal RAWCLK to the clock processing circuit 100. However, since no clock is available inside interface component 10, this transition of NCLKIE will necessarily occur asynchronously to the external clock CLK. Therefore, the signal RAWCLK may. . .

US PAT NO: 5,339,395 [IMAGE AVAILABLE] L12: 2 of 11
US-CL-CURRENT: 395/310; 364/232.9, 239.7, 247.4, 260.1, 270.5, 271, DIG.1; 370/91

ABSTRACT:
An interface circuit is described for interfacing a peripheral device and a microprocessor to enable data transference between a memory location within the peripheral device and a data bus of the microprocessor. In accordance with the type of bus control used by the microprocessor, the interface circuit is operated in either a synchronous mode or an asynchronous mode. The interface includes a state machine that responds to the mode of interface operation, a clock signal provided by the microprocessor, requests from the microprocessor to access an addressed peripheral memory location, and a busy signal from the peripheral device indicating when the peripheral is engaged in transferring data between the interface circuit and an addressed peripheral memory location. Preferably, the interface also operates to detect error conditions based on changes in the access request during data transference between the microprocessor and the peripheral device. In response to detecting an error condition, the state machine acts to interrupt data transference to. . .

SUMMARY:

BSUM(12)

To . . . data transfers between the interface circuit and the microprocessor bus and the interface circuit and the peripheral memory location. The interface circuit also receives a clock signal from the 16:44:32 COPY AND CLEAR PAGE, PLEASE

INPUT:

21 NOV 95 16:46:12 U.S. Patent & Trademark Office P0018

US PAT NO: 5,339,395 [IMAGE AVAILABLE] L12: 2 of 11

BSUM(12)
microprocessor, and an a busy indication from the peripheral device specifying when the peripheral device is engaged in transferring data between the data storage register and the addressed peripheral memory location. In response to the interface operating mode, the request and clock signal received from the microprocessor, and the busy indication received from the peripheral device, the interface circuit operates to control. . .

DETDESC:

DETD(11)

The . . . later point in the specification, input signals such as ADDRESS, R/W*, and CS* are latched into storage locations within bus interface circuit 10 in synchronism with clock signal CLK provided by the host microprocessor 12. The latched values for ADDRESS and R/W* are represented respectively by the. . .

DETDESC:

DETD(41)

The . . . present operating state of the bus interface 10, but with slightly different timings to assure the proper performance of bus interface 10, when the host microprocessor clock (CLK) operates at high speeds.

DETDESC:

DETD(141)

To . . . select the peripheral device for the access (see FIG. 14). Since this all occurs asynchronously with respect to the host clock CLK, the bus interface latches the high to low transition of the CS* signal on the rising edge of the first CLK signal to. . .

CLAIMS:

CLMS(1)

The . . .
is engaged in transferring data between the data storage register and the peripheral memory location; and
control means responsive to the interface operating mode, the clock signal, the request for access from the microprocessor, and the indication of engagement in data transference from the peripheral device,. . .

CLAIMS:

CLMS(3)

3. . . .
engaged in data transference between the temporary data storage register a the peripheral memory location; and
control means responsive to the interface operating mode, the clock signal, the select signal, the read/write signal, and the busy signal for
16:46:13 COPY AND CLEAR PAGE, PLEASE

INPUT:

21 NOV 95 16:46:28 U.S. Patent & Trademark Office P0019

US PAT NO: 5,339,395 [IMAGE AVAILABLE] L12: 2 of 11

CLMS(3)
separately timing and controlling (A) data transference between. . .

CLAIMS:

CLMS(9)

9. . . .
multiple bytes of data between the temporary data storage register and the peripheral memory location; and
control means responsive to the interface operating mode, the clock signal, the select signal, the read/write signal, and the busy signal for separately timing and controlling multiple transference of single. . .

CLAIMS:

CLMS(10)

10. The interface circuit as described in claim 9, wherein the control means further includes:
a state machine responsive to the interface operating mode, the clock signal, the select signal, the read/write signal, and the busy signal for operating the interface circuit in successive interface operating. . .

US PAT NO: H 1,291 [IMAGE AVAILABLE] L12: 3 of 11
US-CL-CURRENT: 395/800, 309, 375

ABSTRACT:
A microprocessor having a memory coprocessor (10) connected to a MEM interface (16) and a register coprocessor (12) connected to a REG interface (14). The REG interface (14) and MEM interface (16) are connected to independent read and write ports of a register file (6). An Instruction Sequencer (7) also connected to an independent write port of the register file, to the REG interface and to the MEM interface. An Instruction Cache (9) supplies the instruction sequencer with at least two instruction words per clock (7). Single-cycle coprocessors (4) are connected to the REG interface (14) and a multiple-cycle coprocessors (2) are connected to the REG interface (14). An Address Generation Unit (3) is connected to the MEM interface (16) for executing load-effective-address instructions and address computations for loads and stores to thereby perform effective address calculations in parallel. . . The Instruction Sequencer (7) decodes incoming instruction words form the Cache, and issues up to three instructions on the REG interface (14), the MEM interface (16), and/or the branch logic within the Instruction Sequencer. The instruction sequencer includes means for detecting dependencies between the instructions to thereby prevent collisions between instructions. A local register cache (5) is provided connected to the MEM interface. The local register cache maintains a stack of multiple word local register sets, such that one each call the local. . .

DETDESC:

DETD(30)

The . . . This allows 528 MB/sec to be transferred each way between the core processor and the memory subsystem. One instruction per clock can be
16:46:28 COPY AND CLEAR PAGE, PLEASE

INPUT:

21 NOV 95 16:46:45 U.S. Patent & Trademark Office P0020

US PAT NO: H 1,291 [IMAGE AVAILABLE] L12: 3 of 11

DETD(30)
issued on this interface. The operations can be single or multi-cycle just as described above for the REG coprocessors. The coprocessors on this interface. . .

DETDESC:

DETD(67)
Clock interface.

DETDESC:

DETD(72)

The Clock Interface

DETDESC:

DETD(73)

This interface is the chip clock phases for a clock as described in Imel U.S. Pat. No. 4,816,700. The system uses the overlapped clock phases to. . .

CLAIMS:

CLMS(1)

What . . .
instruction decoder within said instruction sequencer (7) being capable of decoding multiple instructions and issuing, multiple instructions during a single clock cycle on said REG interface, said MEM interface and said branch logic;
first coprocessors (2,4,12) connected in parallel to said REG interface for receiving first instructions. . .

US PAT NO: 5,274,786 [IMAGE AVAILABLE] L12: 4 of 11
US-CL-CURRENT: 395/421.08; 364/239.3, 254.2, 927.97, 957.5, 968, 968.1, DIG.1, DIG.2; 395/500, 800

ABSTRACT:
An interface unit which can reduce the hardware cost by interfacing a microprocessor with an inexpensive memory device with a smaller word size without compromising the overall performance. The current invention improves the overall performance of the interface system by reducing the overhead address relatching without adding expensive and sophisticated pieces of hardware. This is accomplished by comparing. . . previous address. When a current address contains the same row address as the previously accessed memory-page, the current invention saves clock cycles by avoiding relatching of the row address portion of the address in the memory device. Such saving is significant. . .

SUMMARY:

BSUM(14)

16:46:47 COPY AND CLEAR PAGE, PLEASE

INPUT:

21 NOV 95 16:46:58 U.S. Patent & Trademark Office P0021

US PAT NO: 5,274,786 [IMAGE AVAILABLE] L12: 4 of 11

BSUM(14)
The invention provides an apparatus and a method which minimize address latching so as to save clock cycles in an interface between a microprocessor and a memory device. By so reducing the number of address latches necessary, overhead may be reduced.

DETDESC:

DETD(4)

The interface apparatus of FIG. 2 saves clock cycles during address latching in accordance with the invention as follows. During i860 read and write cycles, controller 108 controls. . .

US PAT NO: 5,210,858 [IMAGE AVAILABLE] L12: 5 of 11
US-CL-CURRENT: 395/550, 250, 445, 494

ABSTRACT:
A clocking control circuit for a computer system and method for receiving a microprocessor clock signal which drives a microprocessor and for supplying a support clock signal having a lower frequency. The support clock frequency drives support interface circuitry such as a peripheral controller, a CPU/memory controller, and a bus bridge interface, and thus causes the support interface circuitry to operate at a lower frequency than the microprocessor. The clocking control circuit ensures synchronization between the support clocking signal and the microprocessor clocking signal. The transmission of control signals between the microprocessor and support interface circuitry is controlled to ensure proper communications between the microprocessor and support circuitry.

SUMMARY:

BSUM(18)

The . . . comprise means for receiving a first clock signal which drives the microprocessor and cache controller and for supplying a support clock signal which drives support interface circuitry having a lower frequency than that of the first clock signal. The clocking control circuit preferably includes a means. . .

CLAIMS:

CLMS(1)

We . . .
and
means for receiving a clock signal which drives said microprocessor and said cache controller and for supplying to said support interface circuitry a support clock signal having a frequency lower than that of said clock signal.

CLAIMS:

CLMS(6)

6. . . .
interface circuitry from said cache controller; and
16:47:00 COPY AND CLEAR PAGE, PLEASE

INPUT:

21 NOV 95 16:47:22 U.S. Patent & Trademark Office P0022

US PAT NO: 5,210,858 [IMAGE AVAILABLE] L12: 5 of 11

CLMS(6)
decreasing the time duration of signals transmitted to said cache controller from said support interface circuitry;
receiving a first clock signal which drives said microprocessor and said cache controller; and
supplying a support clock signal to said support interface circuitry having a frequency lower than that of said first clock signal.

US PAT NO: 4,853,841 [IMAGE AVAILABLE] L12: 6 of 11
US-CL-CURRENT: 395/550; 364/222.2, 229, 229.1, 239, 239.1, 260, 260.1, 270, 270.2, 284, DIG.1

ABSTRACT:
An arrangement, for adapting the serial interface of a data processing system to the data speed of a communication partner, has a recognition circuit for recognizing the. . . unknown transmission speed are inputted to a frequency counter of the recognition circuit and the resulting count provided to a microprocessor which calculates an adjustment division signal N from the counting results. The adjustment divison signal N is inputted to a frequency divider of a phase lock loop (PLL) circuit of an adjustment circuit to provide a divided clock frequency signal which is compared with a divided reference frequency signal by the PPL circuit so that the frequency of a voltage control oscillator of the PLL circuit is adjusted until the divided clock frequency signal and divided reference frequency signal are equal. The adjusted voltage control oscillator signal is inputted to the microprocessor from which a matching data transmission speed equal to the data transmission speed of the communication partner is calculated.

DETDESC:

DETD(18)

When . . . so that the first microprocessor system 2, if it has a joint system clock for the microprocessor and the serial interface can be admitted with a clock frequency signal "ftakt" required for its operation. This is necessary because an operation of the phase locking loop 19 is. . .

DETDESC:

DETD(21)

In a microprocessor system 2 in which only the data transmission of the serial interface is supplied with the clock frequency signal "ftakt", and the microprocessor of the microprocessor system 2 is equipped with its own system clock generator, an. . .

US PAT NO: 4,635,260 [IMAGE AVAILABLE] L12: 7 of 11
US-CL-CURRENT: 371/20.2, 3; 375/213; 395/184.01

ABSTRACT:
A . . . sequence. Eight status parameters are detected at each repeater and monitored at the supervisory terminal. The supervisory terminal includes a clock generator, a receiver-transmitter interface, a microprocessor for processing repeater status information, a display, a selector and a bus interface. Each repeater includes a local oscillator, an error detector, an error counter, a detector of the error counter status, an. . .
16:47:24 COPY AND CLEAR PAGE, PLEASE

INPUT:

21 NOV 95 16:47:44 U.S. Patent & Trademark Office P0023

US PAT NO: 4,635,260 [IMAGE AVAILABLE] L12: 7 of 11

SUMMARY:

BSUM(12)

In . . . error counter overflow, 64-640 errors, 8-63 errors, 4-7 errors, 1-3 errors and 0 errors). The centralized supervisory terminal includes: a clock generator, a receiver-transmitter interface, an information computer or microprocessor, a display and, optionally, a digital selector and a bus interface. The telemetry device connected. . .

US PAT NO: 4,539,655 [IMAGE AVAILABLE] L12: 8 of 11
US-CL-CURRENT: 395/280; 340/825.01; 364/916, 916.2, 919, 919.1, 919.5, 921, 921.4, 921.8, 921.9, 925.6, 926, 926.1, 926.3, 926.7, 926.9, 926.91, 927.2, 927.3, 927.4, 927.6, 927.8, 929, 929.1, 929.2, 929.3, 931, 931.1, 931.4, 931.43, 931.45, 933, 934, 934.2, 934.3, 934.4, 935, 935.1, 935.2, 935.3, 935.4, 935.54, 935.6, 935.7, 937.1, 937.4, 939, 939.4, 939.5, 940, 940.3, 940.4, 940.5, 940.61, 940.64, 940.81, 941, 941.3, 941.7, 942, 942.1, 942.3, 942.4, 942.7, 942.8, 943.9, 943.91, 943.92, 944.2, 944.5, 944.7, 945, 945.4, 945.7, 946.2, 946.6, 947, 947.1, 948.1, 948.4, 949, 949.1, 949.3, 950, 950.1, 950.2, 950.5, 955, 955.6, 958.5, 959, 959.1, 960, 960.2, 964, 965, 965.76, 965.8, DIG.2

ABSTRACT:
A . . . of a master host computer, network processing nodes for monitoring and control of work locations and a subhost node which interfaces the nodes and host computer. The subhost includes dual microprocessor configurations on a common bus, one for communications and one for control, operating 180.degree. out of phase. Each node can. . . display terminals and the like in accordance with system requirements. The nodes communicate via two fiber optic channels, one operating clockwise and the other counterclockwise with foldback capability in the event of a fault. A conventional signal back-up is also provided.

DETDESC:

DETD(39)

PTM 62 provides three independent programmable timer/counters, one of which may be used by the RS-232-C interface 95 as the data transfer clock.

DETDESC:

DETD(40)

The RS-232 communications port 95 working with the PTM 62 or an externally generated baud rate clock input, interfaces this module with the outside world. Communications port 95 consists of a asychronous communications interface adapter (ACIA) and the associated. . .

DETDESC:

DETD(76)

The . . . communications port 151, working with the baud rate generator, 16:47:45 COPY AND CLEAR PAGE, PLEASE

INPUT:

21 NOV 95 16:48:06 U.S. Patent & Trademark Office P0024

US PAT NO: 4,539,655 [IMAGE AVAILABLE] L12: 8 of 11

DETD(76)
the programmable timer (PTM) 153 or an externally generated baud rate clock input 176, interfaces this module with the outside world. The communications port 151 consists of an asynchronous communications adapter (ACIA) and associated level. . .

DETDESC:

DETD(78)

The real time delay circuit 155 provides the time delay required to interface the real time clock/calendar 154 device with the onboard microprocessor. This time delay in accessing the real time clock allows for the difference in. . .

US PAT NO: 4,398,265 [IMAGE AVAILABLE] L12: 9 of 11
US-CL-CURRENT: 395/882; 364/919, 919.2, 919.4, 925.6, 926.1, 926.5, 927.2, 927.5, 927.8, 927.92, 927.98, 927.99, 928, 929, 931.3, 933, 933.2, 933.3, 935, 935.2, 935.3, 935.4, 935.6, 940, 940.1, 940.2, 942.7, 942.8, 946.2, 946.6, 947, 947.1, 948.1, 950, 950.3, 959.1, 964, 964.1, 965, 965.5, 965.8, DIG.2; 455/73

ABSTRACT:
A unique interface adapter is coupled to a microprocessor by a three-wire self-clocking serial data bus for accommodating a twenty-key keyboard and an eight-digit display. The interface adapter includes circuitry for recovering a clock signal and a non-return-to-zero (NRZ) data signal from the data signal transmitted on two forward signal lines of the serial. . .

SUMMARY:

BSUM(5)

In . . . parallel, a large number of interconnections are required. In addition, clock and timing signals must also be connected to such interface adapters for proper operation. Separate clock and timing signals render the reception of data signals by these interface adapters highly susceptible to falsing due to speed. . .

US PAT NO: 4,315,308 [IMAGE AVAILABLE] L12: 10 of 11
US-CL-CURRENT: 395/853; 364/228.6, 232.7, 232.8, 238.3, 238.4, 240, 240.1, 240.2, 240.5, 240.9, 244, 244.6, 254.9, 276.5, 276.8, 284, 284.3, DIG.1

ABSTRACT:
An interface between a microprocessor chip and input/output, and memory modules. The interface uses a single, bidirectional bus comprised of a number of lines which is less than the number necessary to carry. . . or a full width data word. Information transfer is effected by transferring information in small portions utilizing two or more interface clock cycles. An encoded control specification placed on the bus during the first cycle of information transfer specifies the type of. . . transfer, and the length (number of bytes) of data to be moved. Only two additional simplex lines, one from the microprocessor and the other to the microprocessor are needed to complete the basic interface.
16:48:06 COPY AND CLEAR PAGE, PLEASE

INPUT:

21 NOV 95 16:48:32 U.S. Patent & Trademark Office P0025

US PAT NO: 4,315,308 [IMAGE AVAILABLE] L12: 10 of 11

SUMMARY:

BSUM(6)

The . . . read and write input/output and memory operations, thus resulting in reduced pin requirements. In addition to a line carrying system clock signals, a typical microprocessor interface would include the following lines:

US PAT NO: 4,050,096 [IMAGE AVAILABLE] L12: 11 of 11
US-CL-CURRENT: 395/494; 364/225, 229, 229.2, 230, 230.3, 230.4, 232.7, 232.8, 238.3, 238.5, 240.1, 241.2, 241.5, 242.1, 243, 243.3, 243.4, 244, 244.3, 244.6, 245, 245.1, 246, 246.3, 252.3, 252.6, 254, 254.4, 254.5, 254.8, 255, 255.1, 255.2, 255.5, 259, 259.4, 259.7, 261.3, 261.5, 263.2, 264, 264.6, 265, 265.3, 270, 270.3, 270.5, 270.6, 271.5, 271.6, 271.8, 273.4, DIG.1

ABSTRACT:
A digital system comprises a plurality of metal-oxide-semiconductors (MOS) chip random access memory (RAM) and read only memory (ROM) and peripheral interface adaptor circuits used as part of the computer coupled to a common bidirectional data bus which is coupled to and controlled by a microprocessor unit (MPU) chip. In the digital system, data transfers on the common bidirectional data bus are accomplished without the use. . . when the memory is ready to transfer data is not required. This is accomplished by logic circuitry which expands a clock signal pulse which is applied to the microprocessor chip whenever a memory location is addressed which has a longer access time than is consistent with the width of the pulse ordinarily applied to the microprocessor to effect its operation.

DETDESC:

DETD(205)

The Microprocessor Unit (MPU) may be configured with a Read Only Memory (ROM), Random Access Memory (RAM), a Peripheral Interface Adapter (PIA), restart circuitry and clock circuitry to form a minimum functional system, as shown in FIG. 11). Such a system can easily be adapted for. . .

=> d his

(FILE 'USPAT' ENTERED AT 16:21:54 ON 21 NOV 95)
SET PAGELENGTH 62
SET LINELENGTH 78

L1	26522	S 395/?/CCLS
L2	1403	S L1 AND (MICROPROCESSOR?)/AB
L3	2	S L2 AND (RING (5A) COUNTER (5A) CLOCK?)
L4	7	S L2 AND (COUNTER (5A) CLOCK?)/AB
L5	28	S L1 AND (MICROPROCESSOR? (5A) COUNTER (5A) CLOCK?)
L6	6	S L1 AND (MICROPROCESSOR? (5A) VARIABLE (5A) CLOCK?)
L7	65	S L1 AND (RING (5A) COUNTER (5A) CLOCK?)
L8	2	S L7 AND MICROPROCESSOR?/AB
L9	3	S L1 AND (CIRCULAR (5A) COUNTER (5A) CLOCK?)
L10	1403	S L1 AND MICROPROCESSOR?/AB
L11	78	S L10 AND INTERFACE? (5A) CLOCK

16:48:43 COPY AND CLEAR PAGE, PLEASE

INPUT:

21 NOV 95 16:48:59 U.S. Patent & Trademark Office P0026
L12 11 S L11 AND (INTERFACE? AND CLOCK?)/AB

=>

INPUT: